Application Note

Document No.: AN1106

APM32F411xCxE Hardware Development Guide

Version: V1.0

1 Introduction

This application note provides minimum hardware design specifications for the APM32F411xCxE series, including power supply schemes, clock sources, reset methods, startup configurations, and debugging management. Detailed reference designs, including explanations of primary components, interfaces, and modes, are also included in this document.

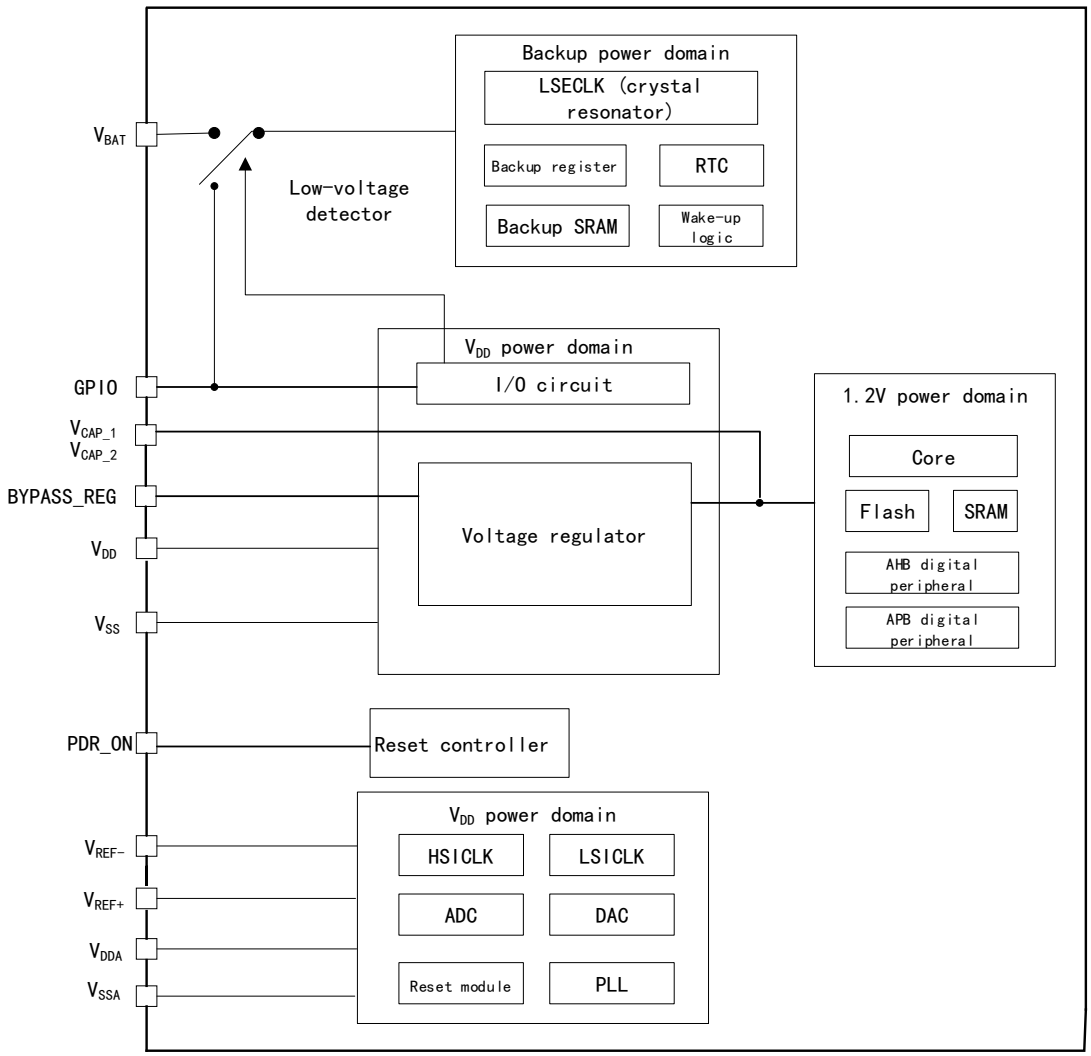
Contents

2 Power supply

2.1 Overview

The power supply is the basis for the stable operation of a system. The working voltage is 1.8~3.6V. It can provide a 1.2V power supply through the built-in voltage regulator. If the main power V_{DD} is powered down, it can supply power to the backup power supply area through V_{BAT}.

Figure 1 Power Supply Control Structure Block Diagram



2.1.1 Voltage regulator

Power can be supplied to 1.2V power domain in the following operating modes:

- Normal mode: In this mode, 1.2V power supply area operates at full power.
- Stop mode: In this mode,1.2V power supply area works in low-power state, all clocks are disabled, peripherals stop working.

- Standby mode: In this mode, 1.2V power supply area stops power supply, and except for the standby circuit, the content of register and SRAM will be lost.

2.1.2 Backup power domain

- When V_{DD} exists, the backup power supply area is powered by V_{DD}. When V_{DD} is powered down, the backup power supply area is powered by V_{BAT}, which is used to save the content of backup register and maintain RTC function. Power the LSECLK crystal oscillator, RTC, backup register, RCM_BDCTRL register ,PC13, PC14, PC15 and wake-up logics.
- V_{BAT} must be connected to an external battery when V_{DD} is not in use.

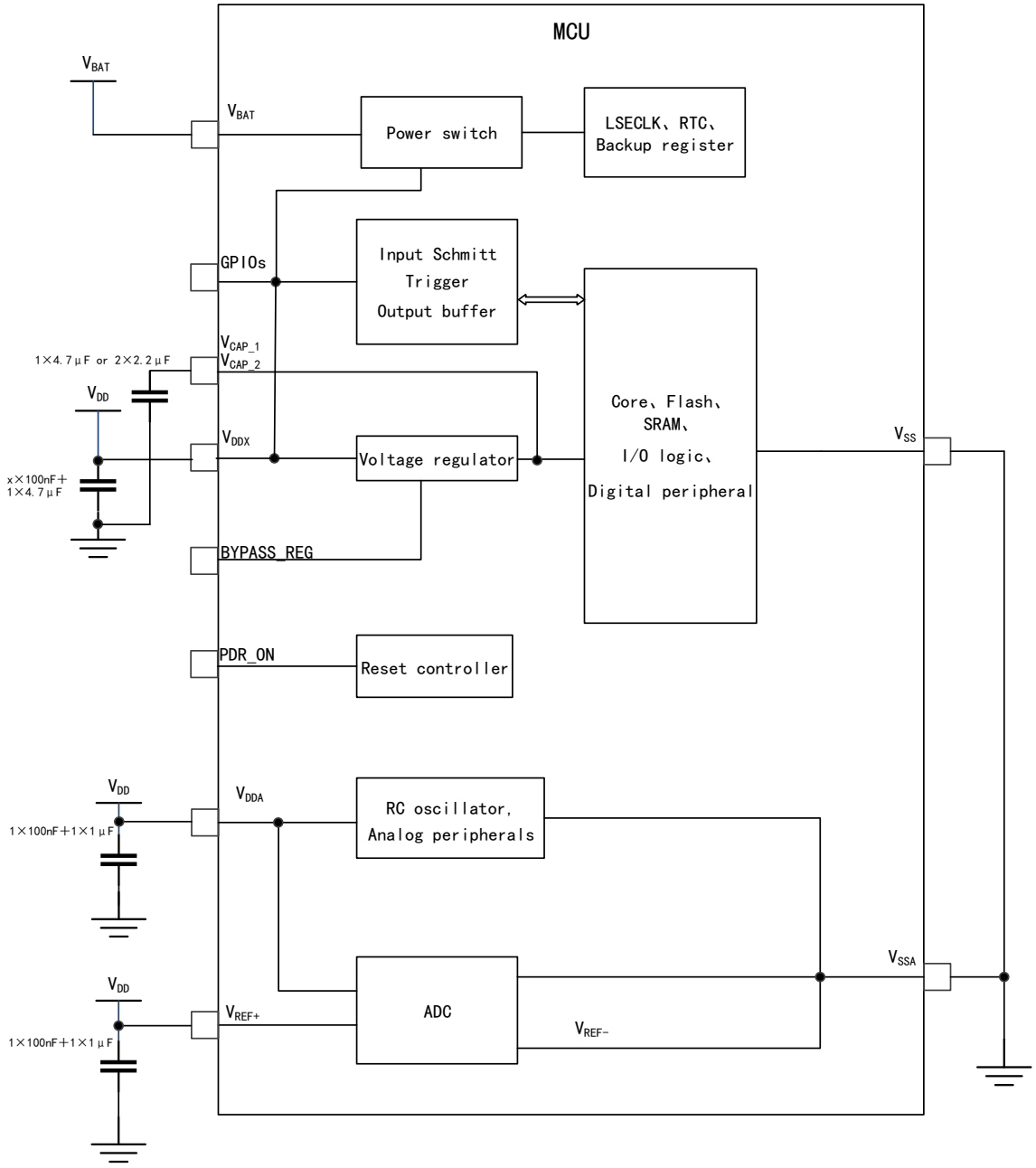
2.1.3 Independent ADC power supply and reference voltage

Independent ADC power supply can improve conversion accuracy, and the specific power pins are as follows:

- V_{DDA}:Power pin of ADC
- V_{SSA}:Independent power ground pin
- V_{REF}+/V_{REF}-:Reference voltage pin of ADC

2.2 Power supply scheme

Figure 2 Power Supply Scheme



Pay attention to the power supply range of each power domain：

Table 1 Power Supply Scheme

Name	Voltage range	Description
V_{DD}	1.8～3.6V	V_{DD} directly supplies power to the IO port, while V_{DD} supplies power to the core circuit through a voltage regulator.
V_{DDA}/V_{SSA}	1.8～3.6V	Supply power to ADC, reset module, RC oscillator and PLL analog part; when ADC is used, V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}

Name	Voltage range	Description
		respectively.
V_{BAT}	1.8V～3.6V	When V_{DD} is disabled, V_{BAT} automatically powers the RTC, external 32KHz oscillator, and backup registers

Where：

Table 2 Precautions for Power Domain

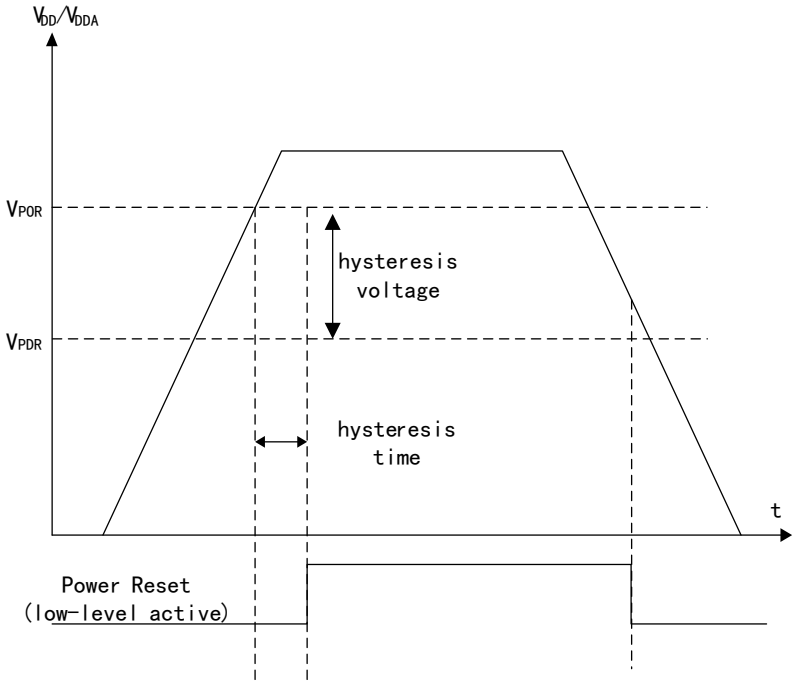
Name	Precautions
V_{DD}	V_{DD} must be connected to external capacitors (x number of ceramic capacitors of 100nF and one tantalum capacitor or ceramic capacitor of no less than 4.7μF) to the V_{DD} power supply.V_{DDx} means that the number of V_{DD} is x.
V_{BAT}	The VBAT pin can be connected to external battery (1.8V < V_{BAT} < 3.6V). If there is no external battery, an external ceramic capacitor of 100nF needs to be connected to the V_{DD} power supply.
V_{DDA}	The VDDA pin must be connected to external capacitor (ceramic capacitor of 10nF + tantalum capacitor or ceramic capacitor of 1μF).
V_{REF+}	The VREF+ pin can be directly connected to V_{DDA} or used separately with external reference voltage. A 10nF and a 1μF capacitor must be connected to this pin. The voltage range for V_{REF+} must be between 1.8V and V_{DDA}.
V_{CAP}	Connecting the external capacitor C_{EXT} to VCAP_1 and VCAP_2 pins to achieve stability of the main voltage regulator. When the regulator is enabled, pins VCAP_1 and VCAP_2 must be connected to two low ESR ceramic capacitors with a rated capacitance of 2.2 μF and an equivalent series resistance (ESR) less than 2Ω, respectively. If certain packages of the microcontroller only provide the VCAP_1 pin, then only this pin should be connected to a low ESR ceramic capacitor with a capacitance of 4.7 μF and ESR less than 1Ω.

2.3 Power supply management and reset

2.3.1 Power-on/power-down reset (POR and PDR)

When the V_{DD}/V_{DDA} is lower than the threshold voltage V_{POR} and V_{PDR}, the chip will automatically remain in the reset state. The waveform diagrams of power-on reset and power-down reset are as follows. For POR, PDR, hysteresis voltage and hysteresis time, please refer to the *Datasheet.*

Figure 3 Power-on Reset and Power-down Reset Oscillogram



2.3.2 Power voltage detector (PVD)

A threshold can be set for PVD to monitor whether V_{DD}/V_{DDA} is higher or lower than the threshold. If the interrupt is enabled, the interrupt can be triggered to process the V_{DD}/V_{DDA} exceeding the threshold in advance. The usage of PVD is as follows:

(1) Set the PVDEN bit of the configuration register PMU_CTRL to 1 to enable PVD

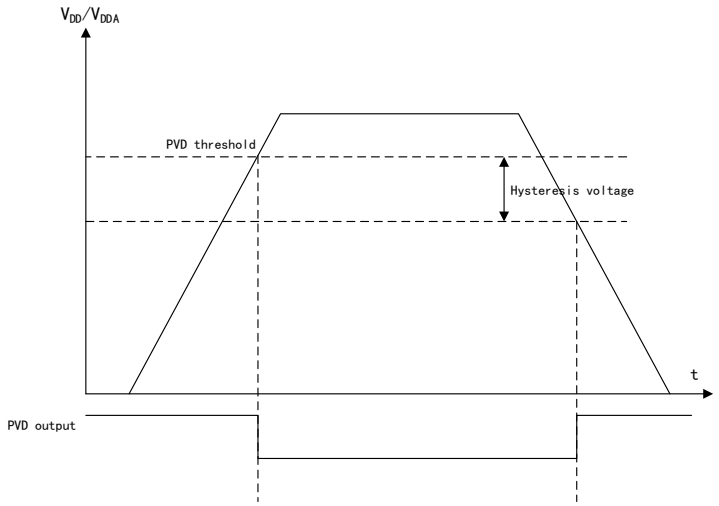
(2) Select the voltage threshold of PVD through the PLSEL[2:0] bit of the configuration register PMU_CTRL

(3) The PVDOFLG bit of the configuration register PMU_CSTS indicates whether the value of V_{DD} is higher or lower than the threshold of PVD

(4) When it is detected that V_{DD}/V_{DDA} is lower or higher than the threshold of PVD, PVD interrupt will be generated

The threshold waveform of PVD is shown below. Please see "*Datasheet*" for PVD threshold and hysteresis voltage.

Figure 4 PVD Threshold Oscillogram



2.3.3 System reset

The reset source is divided into external reset source and internal reset source.

Table 3 Reset Source

Reset source	Description
External reset source	Low level on NRST pin
Internal reset source	（1）Window watchdog termination count (WWDT reset) （2）Independent watchdog termination count (IWDT reset) （3）Software reset (SW reset) （4）Power reset （5）Low-power management reset

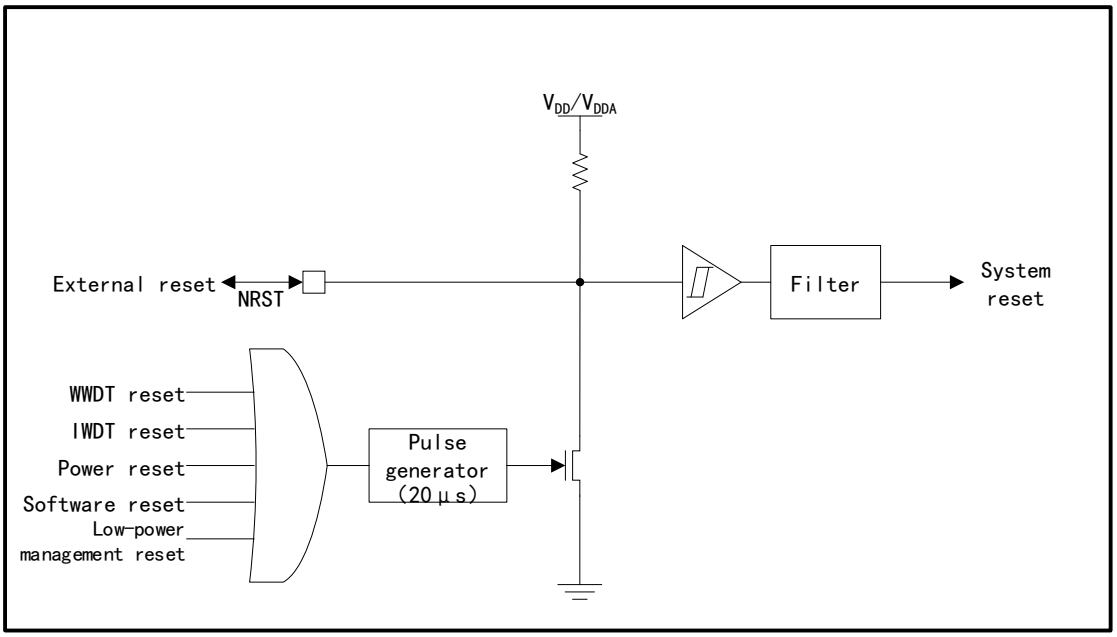
A system reset will occur when any of the above events occur. Besides, the reset event source can be identified by viewing the reset flag bit in RCM_CSTS (control/status register).

2.3.3.1 System reset circuit

The reset source is used in the NRST pin, which remains low in reset process. The internal reset source generates a delay of at least 20μs pulse on the NRST pin through the pulse generator, which causes the NRST to maintain the level to generate reset; the external reset source directly pulls down the NRST pin level to generate reset.

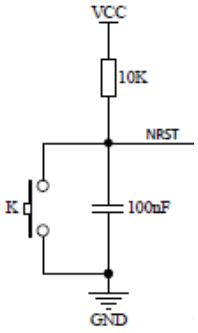
The system reset circuit is shown in the figure below:

Figure 5 System Reset Circuit



Recommended external reset circuit：

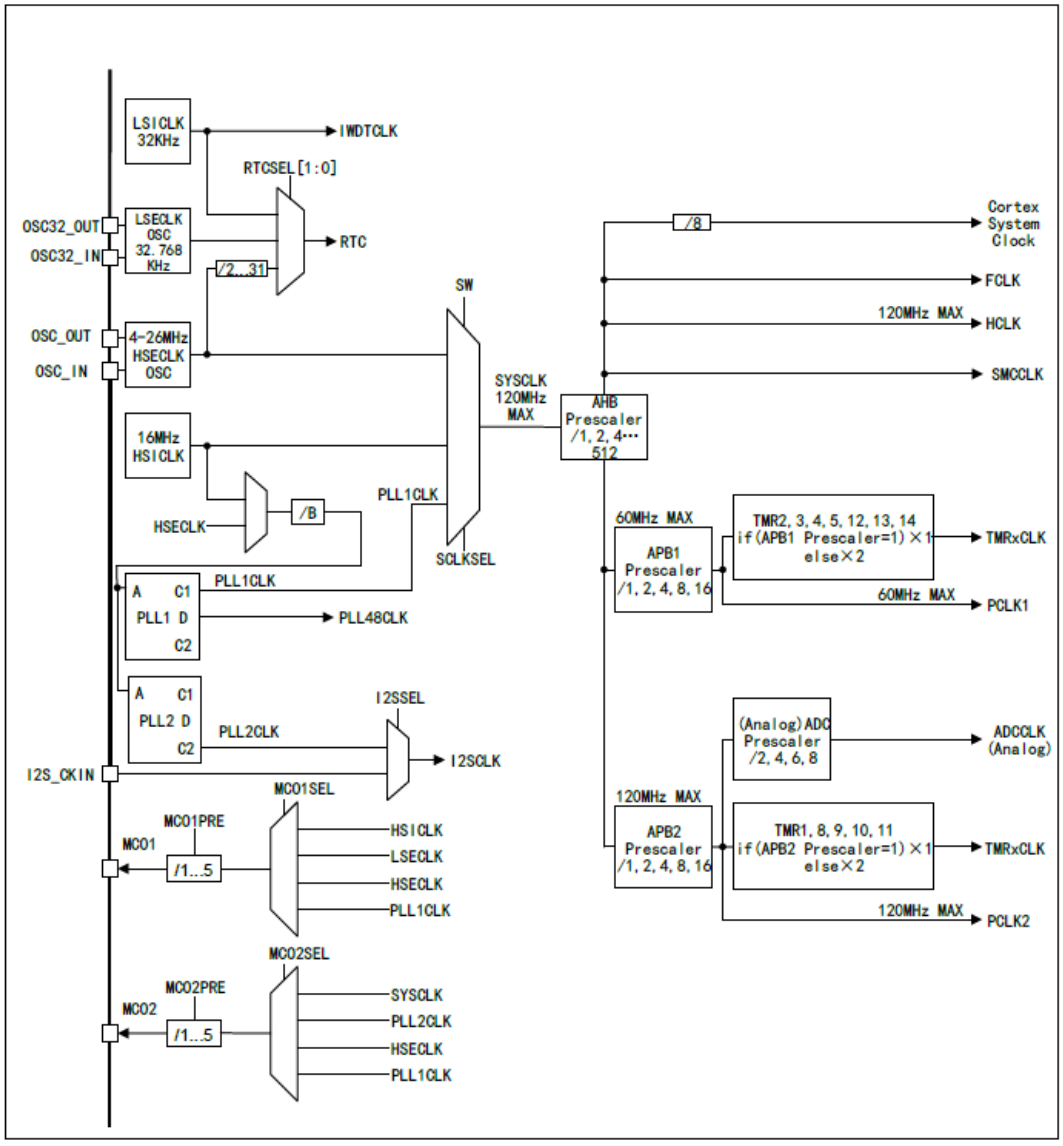
Figure 6 External Reset Circuit



3 Clock

The clock sources for the entire system include HSECLK, LSECLK, HSICLK, LSICLK, PLL. For the characteristics of the clock source, please refer to the relevant chapter of "Electrical Characteristics" in the Datasheet.

Figure 7 Clock Tree



3.1 External clock source

The external clock signal includes HSECLK (high-speed external clock signal) and LSECLK (low-speed external clock signal).

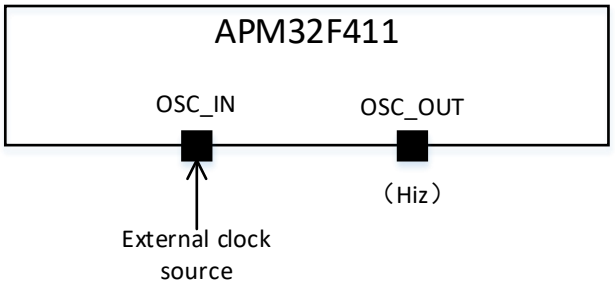
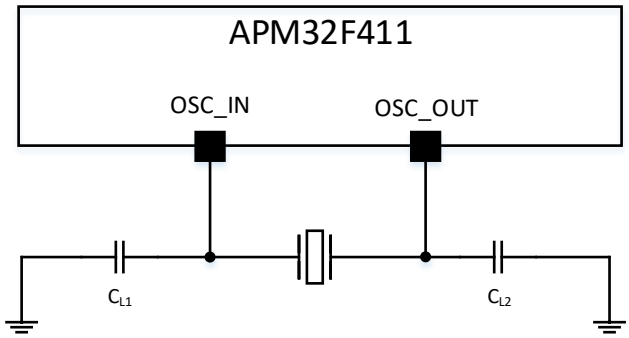
There are two kinds of external clock sources:

- External crystal/ceramic resonator

- External clock of user

The hardware configuration of the two kinds of clock sources is shown in the figure below:

Figure 8 HSECLK/LSECLK Clock Source Hardware Configuration

Clock Source	Hardware Configuration
External clock	
Crystal/ceramic resonator	

Note:

（1）To reduce distortion in clock output and shorten start-up stabilization time, the crystal/ceramic resonator and load capacitors must be placed as close as possible to the oscillator pins. The values of matching capacitances (C_{L1}, C_{L2}) must be adjusted according to the selected oscillator.

（2）The load capacitance C_L follows the formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + Cs$. Cs represents the related capacitance of the PCB and MCU pins, with typical values between 2pF and 10pF.

3.1.1 HSECLK high-speed external clock signal

HSECLK clock signal has two clock sources: HSECLK external crystal/ceramic resonator and HSECLK external clock.

Table 4 Clock Source Generating HSECLK

Name	Description
External clock source (HSECLK bypass)	Provide clock to the MCU through OSC_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle,

Name	Description
	and the maximum frequency is up to 26MHz. For hardware connection, it must be connected to OSC_IN pin, ensuring OSC_OUT pin is suspended.
External crystal/ceramic resonator (HSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency range is 4-26MHz. When OSC_IN and OSC_OUT need to connect to the resonator, it can be enabled and disabled by setting the HSEEN bit in clock control register RCM_CTRL. The formula for the external matching capacitance size is as follows: $C_{L1} = C_{L2} = 2*(C_L - C_S)$, where C_S represents the parasitic capacitance between the PCB and the MCU pins, typically with a value of 10pF. It is recommended to select an external high-speed crystal with a load capacitance of around 20pF. This way, the external matching capacitors C_{L1} and C_{L2} can be 20pF, and during PCB layout, they should be placed as close to the crystal pins as possible, preferably near ground.

3.1.2 LSECLK low-speed external clock signal

LSECLK clock signal has two clock sources: LSECLK external crystal/ceramic resonator and LSECLK external clock.

Table 5 Clock Source Generating LSECLK

Name	Description
External clock source (LSECLK bypass)	The clock is provided to MCU by OSC32_IN pin. The signal can be generated by ordinary function signal transmitter (in debugging), crystal oscillator and other signal generators; the waveform can be square wave, sine wave or triangle wave with 50% duty cycle, and the signal frequency needs to be 32.768kHz. For hardware connection, it must be connected to OSC32_IN pin, ensuring OSC32_OUT pin is suspended; for MCU configuration, the user can select this mode by setting LSEBCFG and LSEEN bits in RCM_BDCTRL (backup domain control register).
External crystal/ceramic resonator (LSECLK crystal)	The clock is provided to MCU by the resonator, and the resonator includes crystal resonator and ceramic resonator. The frequency is 32.768kHz. OSC32_IN and OSC32_OUT need to be connected to the oscillator which can be enabled and disabled through LSEEN bit in RCM_BDCTRL. The formula for the external matching capacitance size is: $C_{L1} = C_{L2} = 2*(C_L - C_S)$, where CS represents the parasitic capacitance between the

Name	Description
	PCB and MCU pins, with a typical value of 5pF. It is recommended to select an external crystal with a load capacitance of around 10pF. This way, the values of the external matching capacitors C_{L1} and C_{L2} can be 10pF, and during PCB layout, they should be placed as close to the crystal pins as possible, preferably near ground.

4 Startup configuration

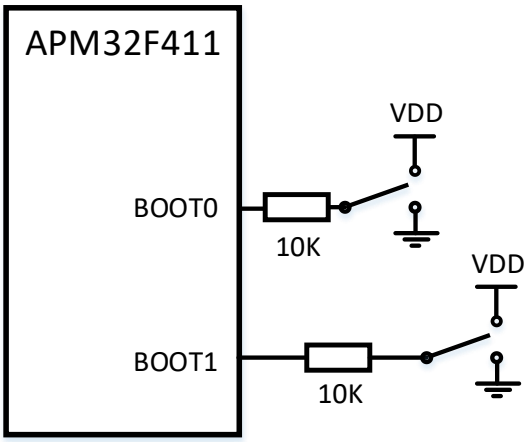
APM32F411xCxE series MCU realizes a special mechanism. By configuring the BOOT[1:0] pin, three different startup modes can be used, and the system can not only start from Flash memory or system memory but also start from the built-in SRAM. The memory selected as the start zone is determined by the selected startup mode.

Table 6 Startup Mode Configuration and Access Mode

Startup mode selection pin		Startup mode	Access methods
BOOT0	BOOT1		
0	X	Main flash memory (Flash)	The main flash memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.
1	0	System memory	The system memory is mapped to the boot space (0x0000 0000), but it can still be accessed at its original address.
1	1	Built-in SRAM	SRAM can be accessed only at the starting address.

- The user can select the startup mode after resetting by setting the state of BOOT1 and BOOT0.
- BOOT pin should keep the startup configuration required by user in standby mode. When exiting the standby mode, the value of boot pin will be latched.
- If you choose to start from built-in SRAM, you must use NVIC's exception table and offset register to remap the vector table to SRAM when writing the application code.

Figure 9 Recommended BOOT Circuit Design



5 Debugging interfaces(SWJ-DP)

The product supports two debugging interfaces: Serial Wire Debug Port (SW-DP) and JTAG Debug Port (JTAG-DP).

Table 7 Debugging Interfaces

Name	Description
SW-DP	The SW-DP interface provides a 2-pin (data + clock) interface for the AHB module. Some of the 2 pins of the SW-DP interface and 5 pins of the JTAG interface are multiplexed
JTAG	The JTAG interface provides a 5-pin standard JTAG interface for AHB access port.

5.1 Debug pin function configuration

- Realize the on-line programming and debugging of the chip.
- Using KEIL/IAR and other software to implement online debugging, downloading and programming.
- Flexible implementation of production of bus-off programmer.

Table 8 Pin Function Configuration

SWJ-CFG[2:0]	Configured as dedicated pin for debugging	I/O port assignment of SWJ interface				
		PA13/ JTMS/ SWDIO	PA14/ JTCK/ SWCLK	PA15/ JTDI	PB3/ JTDO	PB4/ JNTRST
Others	Disable	Release				
100	Both JTAG-DP interface and SW-DP interface disabled					
010	JTAG-DP interface disabled, SW-DP interface enabled	Special	Special	Release		
001	All SWJ pins (JTAG-DP+SW-DP) Except JNTRST pin	Special	Special	Special	Special	Release
000	All SWJ pins (JTAG-DP+SW-DP) Reset state	Special	Special	Special	Special	Special

5.2 IO status during reset and just after reset

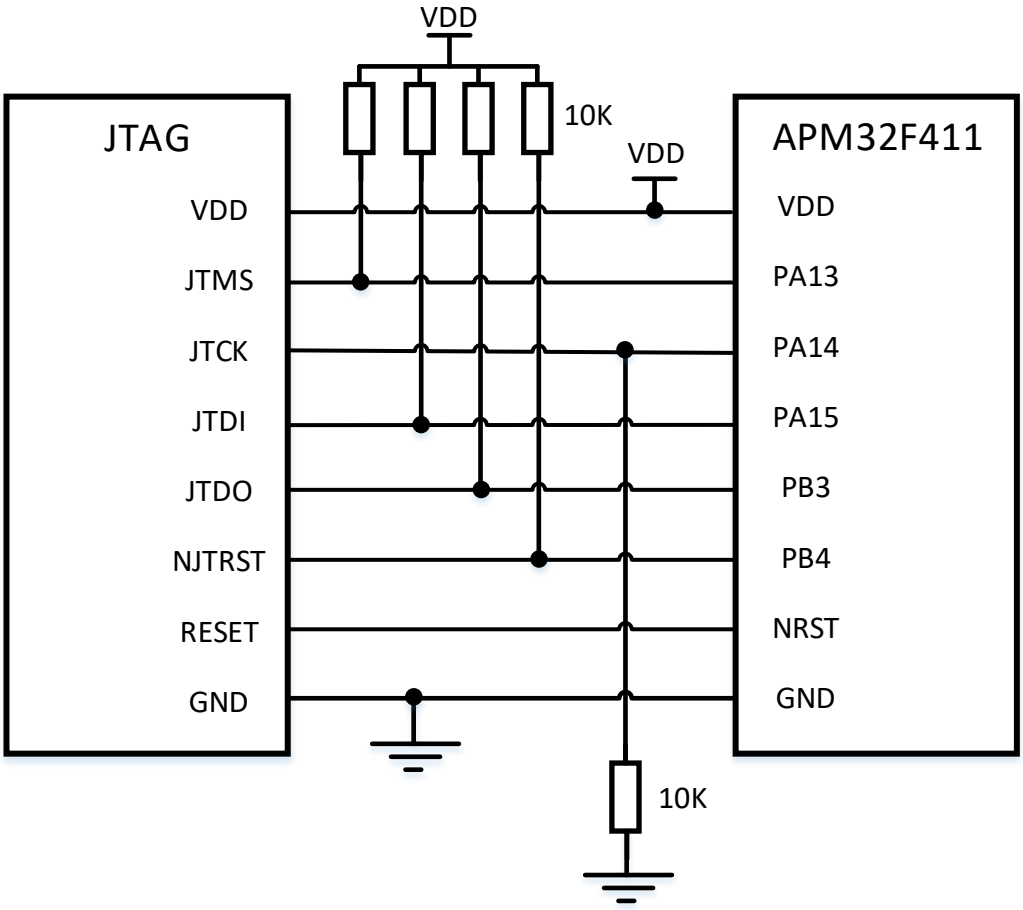
The multiplexing function is not enabled during and just after GPIO reset, the I/O port will be configured as floating input mode, and in such case, the pull-up/pull-down resistor is disabled in input mode. After reset, the JTAG pin is put in the input pull-up or pull-down mode, and the specific configuration is as follows:

- PA15:JTDI in pull-up mode JTDI ;
- PA14:JTCK in pull-down mode;
- PA13:JTMS in pull-up mode;
- PB4: JNTRST in pull-up mode;
- PB3: JTDO is put in floating mode.

5.3 Recommended debugging interface circuit

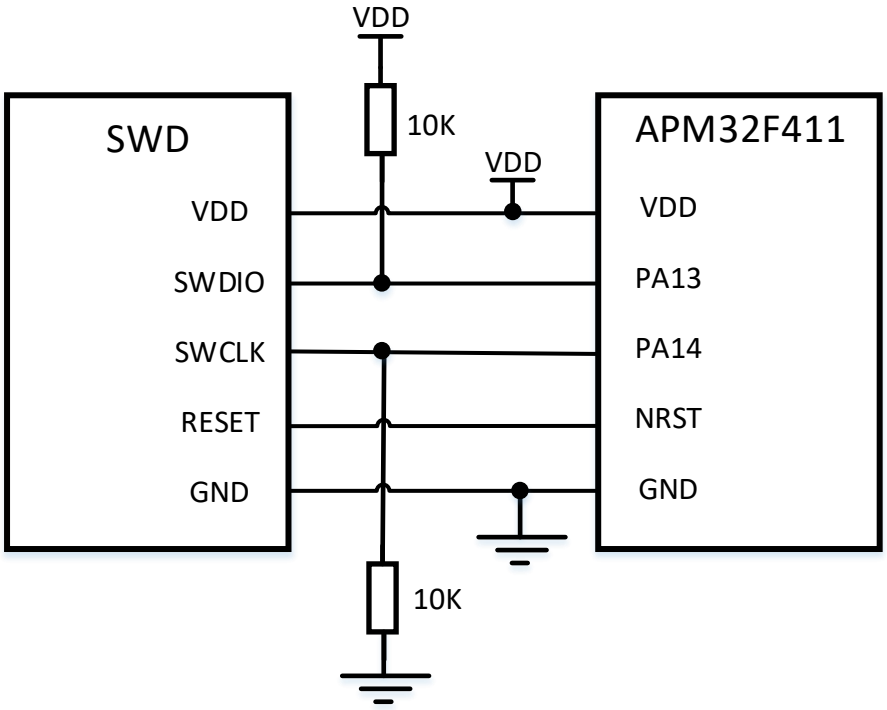
Recommended JTAG Interface Reference Design:

Figure 10 JTAG Interface Circuit



Recommended SWD Interface Reference Design:

Figure 11 SWD Interface Circuit



6 Design recommendations

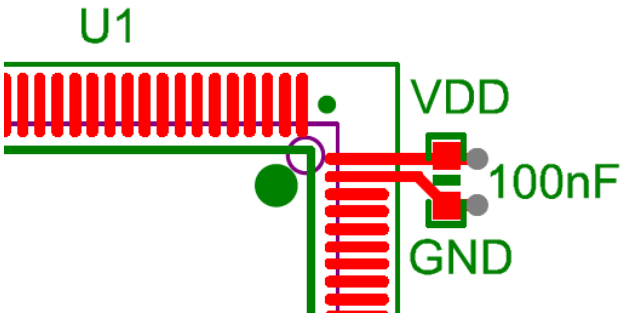
6.1 PCB stack-up

- Number of Layers: It is recommended to use a multi-layer design to ensure independent GND and power layers, which can better guarantee signal integrity and enhance shielding effectiveness. However, for cost considerations, users can reduce the number of layers while ensuring good grounding and power supply.
- Signal and Ground Layers: The signal layer should be adjacent to the ground layer. This helps to reduce electromagnetic interference and the loop area of the signal path, while also serving as a reference plane for the signal.
- Power Supply and Ground Layers: The power supply layer should be separated from the ground layer.

6.2 Power supply design

- Stable power supply input: Ensure stable power supply, the power supply pins should be well filtered, when connecting large capacitance or inductive loads, attention should be paid to ensuring the stability of the power supply design to avoid affecting the power supply stability of the MCU. Measures such as adding filtering capacitors, soft start circuits, and surge protection circuits can be used to ensure the stability of the input power supply.
- Decoupling capacitors: Place one or more 100nF decoupling capacitors near each VDD pin of the chip (depending on the application). (VDD/VDDA/VABT/VREF+) Decoupling capacitors should be placed as close as possible to the relevant pins to achieve the best effect.

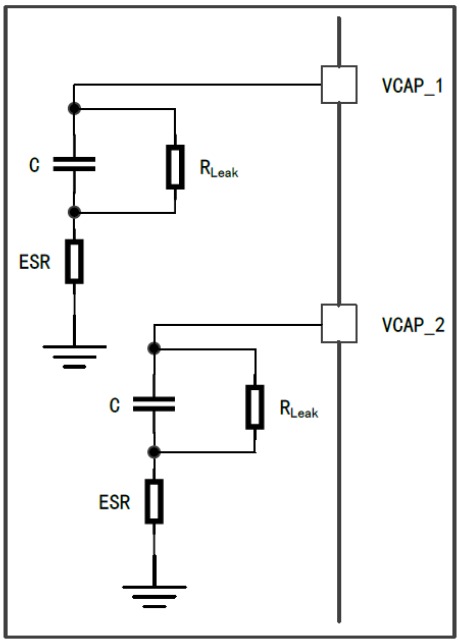
Figure 12 Recommended Layout Design for Decoupling Capacitors for Power Supply Pins



- External capacitors: By connecting the external capacitor C_{EXT} to VCAP_1 and VCAP_2 pins to achieve stability of the main voltage regulator. For cases where only one VCAP pin is supported, a single capacitor can be used instead of two external capacitors C_{EXT}. Among them, ESR is the equivalent series

resistance,R_{leak} is the leakage resistance

Figure 13 External Capacitors C_{EXT}



Note: VCAP_1 and VCAP_2 pins must be connected to 2*2.2 μF LowESR < 2Ω ceramic capacitors (if only VCAP_1 pin is provided on certain packages, then connect to 1*4.7 μF LowESR < 1Ω ceramic capacitor). In PCB layout, external capacitors should be placed close to the VCAP pins (recommended placement distance within 5mm).

- Power supply routing: It is recommended to make the power routing wide and short enough to reduce voltage drop and parasitic parameter effects.

6.3 Grounding

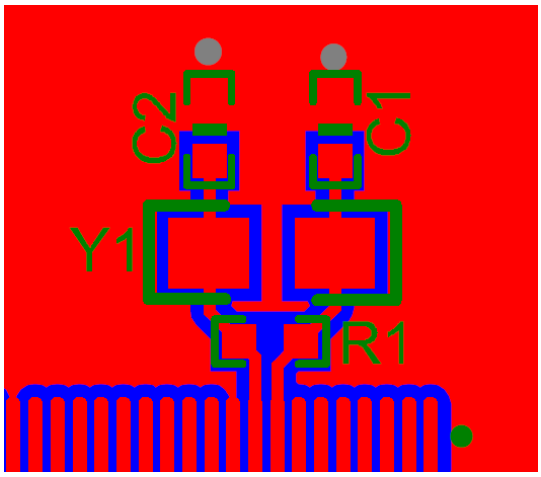
- Single-point grounding: In low-frequency circuits or circuits with low noise requirements, single-point grounding can avoid the formation of ground loops. In this case, all grounding points should be connected to a common grounding point, which is usually the negative pole of the power supply or a grounding plane on the circuit board.
- Multi-point grounding: In high-frequency circuits or high-current circuits, multi-point grounding is typically used. The grounding of each component or functional module is directly connected to the nearest grounding plane, which can reduce the impedance of the ground line, and reduce noise and electromagnetic interference.
- Separation of analog and digital ground: If the MCU processes both analog and digital signals simultaneously, the analog ground and digital ground should be separated. This can be achieved by physically separating the two grounding planes and then merging them at a certain point to connect to the main ground,

reducing the interference of digital noise on the analog signal.

6.4 Clock design

- Crystal oscillator selection: Select a suitable crystal oscillator to ensure that it meets the operating frequency and stability requirements of the MCU.
- Routing recommendations: Clock signal routing should be kept as short as possible and away from high-current, high-speed, and other strong interference signals. It is also recommended to use ground stitching to enhance shielding effectiveness.
- Layout recommendations: The crystal oscillator circuit should be placed close to the chip and on the same layer as the chip. To reduce interference, it is best to have a complete ground plane beneath the entire crystal oscillator circuit.

Figure 14 Recommended Clock Pin Layout Design



6.5 I/O design

- I/O configuration: Correctly configuring the mode of I/O ports, such as input, output, pull-up, pull-down, and open-drain.
- Protection: For externally connected I/O ports, consider adding voltage protection (TVS/ESD diodes) and series resistors.
- For some pins connected to internal analog channels, these pins are sensitive to negative voltage. In extreme cases, negative voltage may cause the MCU system to reset. It is recommended to implement IO filtering and protection design when using these pins.

6.6 EMC and EMI

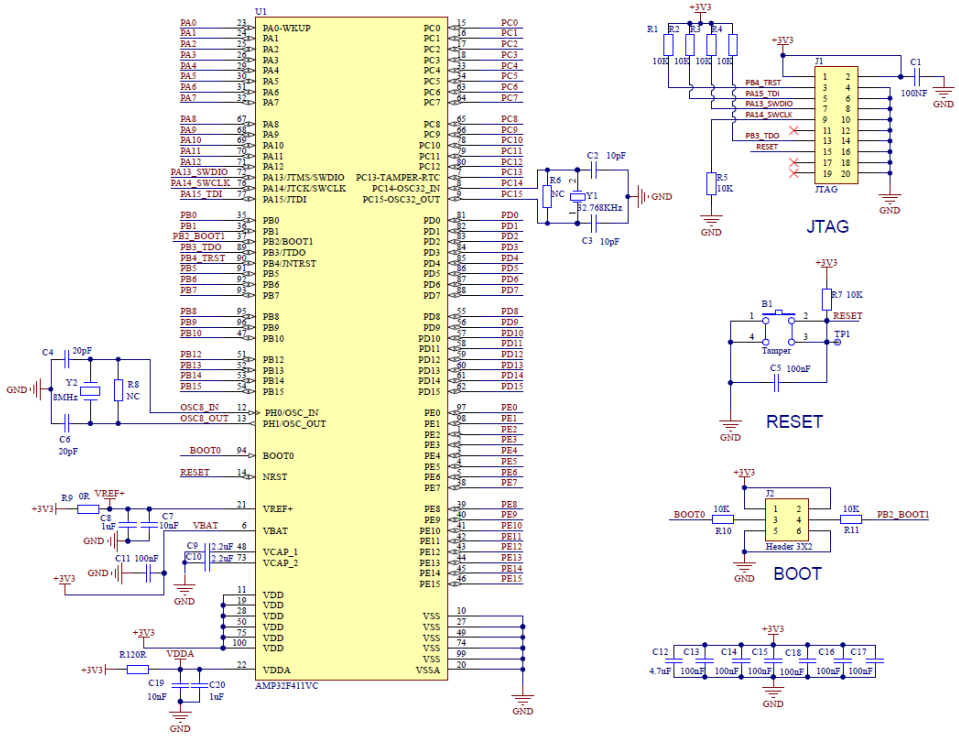
- Layout: Consider electromagnetic compatibility (EMC) and electromagnetic interference (EMI) in the design. The layout should be reasonable. For example, when laying out the MCU circuit, it should be far away from high-power and strong interference sources, and the loop area should be minimized when routing. Low-

frequency small signals should be kept away from high-frequency signals and large current loops

- Shielding: Use shielding and reasonable grounding strategies for sensitive and high-speed circuits.

6.7 Reference schematic design

Figure 15 Reference Schematic



7 Revision History

Table 9 Document Revision History

Date	Version	Change History
2024.1.23	V1.0	New

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8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.